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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/347,409 | 07/06/1999 | TETSUYA AKIMOTO | Q55026 | 3821 |

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| EXAMINER |
|---|
| DAY, HERNG-DER |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | 5 |

DATE MAILED: 06/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/347,409 | AKIMOTO ET AL. | |
| | Examiner | Art Unit | |
| | Herng-der Day | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. Claims 1-12 have been examined.

### *Priority*

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10-190685, filed on 7/6/98.

### *Information Disclosure Statement*

3. The information disclosure statement filed 10/11/2000 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to has not been considered.

### *Drawings*

4. The drawings are objected to because the drawings do not match the specification. Specifically, the specification states: "the delay time degradation rate calculation 105 is carried out on the basis of input pin information 102," as described in lines 6-7 of page 2. However, no relationship is shown between 105 and 102 in Fig. 1. A proposed drawing correction or

corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

5. The title of the invention is currently directed to non-statutory subject matter. A new title is required that is clearly indicative of the invention to which the claims are directed.

6. The disclosure is objected to because of the following informalities:

(a) "propagation velocity $t_{pd}$" in line 15 of page 8 is inconsistent with the description of "transmission delay time" in line 17 of page 16. It appears that "propagation velocity $t_{pd}$" in line 15 of page 8 should be "propagation delay time $t_{pd}$".

(b) "$W_{in}$" in line 16 of page 10 has a different definition from "$W_{in}$" in line 5 of page 10. It appears that "$W_{in}$" in line 16 of page 10 should be "$W_{out}$".

(c) "the delay time degradation rate calculation 305" in line 12 of page 12 does not match drawing Fig. 3. It appears that "the delay time degradation rate calculation 305" in line 12 of page 12 should be "the delay time degradation rate calculation 308".

(d) "frequency T" in line 13 of page 15 is inconsistent with "f=1/T" in line 6 of page 16. It appears that "frequency T" in line 13 of page 15 should be "period T".

(e) At page 16, line 17, "Fig. 4" does not show a transmission delay time in the inverter. However, it is noted that Fig. 5 does show a transmission delay time in the inverter. It appears that "Fig. 4" in line 17 of page 16 should be "Fig. 5".

Appropriate correction is required.

### *Claim Objections*

7. Claim 4 is objected to because of the following informalities: at page 23, line 3, "calculating an amount of stress $S_{in}$ cast by the input pin and and an amount of stress $S_{out}$ cast by the output pin". (Emphasis added.) Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

8. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8.1 Claims 1-12 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter.

8.2 Regarding claim 1, this claim is directed to "a method of calculating, by the use of a computer, a numerical value", and the steps recited in claim 1 describe mathematical algorithms comprising the abstract idea of calculating a numerical value $V_A$. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.3 Regarding claim 2, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 1 above.

8.4 Regarding claim 3, this claim is directed to "a method of calculating, by the use of a computer, a pin-to-pin delay time and a block-to-block delay time", and the steps recited in claim 3 describe mathematical algorithms comprising the abstract idea of calculating delay times. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.5 Regarding claim 5, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 3 above.

8.6 Regarding claim 4, this claim is directed to "a method of calculating, by the use of a computer, pin-to-pin delay time and block-to-block delay time", and the steps recited in claim 4 describe mathematical algorithms comprising the abstract idea of calculating delay times. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.7 Regarding claim 6, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a

practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 4 above.

8.8 Regarding claim 7, this claim is directed to "a computer software product for calculating a numerical value", and the steps recited in claim 7 describe mathematical algorithms comprising the abstract idea of calculating a numerical value $V_A$. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.9 Regarding claim 8, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 7 above.

8.10 Regarding claim 9, this claim is directed to "a computer software product for calculating a pin-to-pin delay time and a block-to-block delay time", and the steps recited in claim 9 describe mathematical algorithms comprising the abstract idea of calculating delay times. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.11 Regarding claim 11, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a

practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 9 above.

8.12 Regarding claim 10, this claim is directed to "a computer software product for calculating pin-to-pin delay time and block-to-block delay time", and the steps recited in claim 10 describe mathematical algorithms comprising the abstract idea of calculating delay times. These steps do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of any output to a practical application providing a useful, concrete, and tangible result.

8.13 Regarding claim 12, the limitations supplied in these claims do not: (1) recite data gathering limitations or post-mathematical operations that might independently limit the claims beyond the performance of a mathematical operation; or (2) limit the use of the output to a practical application providing a useful, concrete, and tangible result. The analysis and conclusion regarding non-statutory subject matter is identical to claim 10 above.

### *Claim Rejections - 35 USC § 102*

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined

was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-3, 5, 7-9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwanishi et al., U.S. Patent 6,047,247 issued April 4, 2000.

10-1. Regarding claims 1 and 7, Iwanishi et al. disclose a method of calculating a numerical value $V_A$ representative of a circuit property of a logic level circuit, from a numerical value $V_B$, which shows a block property of a logic block included in the logic level circuit (a delay calculation step, column 6, lines 35-40), comprising the steps of:

(a) calculating the $V_B$ (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from numerical values $V_C$'s (circuit information of the LSI, delay library containing delay parameters, column 6, lines 37-38) each of which represents a transistor property of a transistor included in the logic block; and,

(b) calculating the $V_A$ (delay calculation of an LSI, column 6, lines 35-36) from the $V_B$.

10-2. Regarding claims 2 and 8, Iwanishi et al. further disclose a delay calculation step, column 6, lines 47-51, wherein, each $V_C$ (input slew, column 6, line 48) shows a specific one of the transistor property of the transistor connected to an input pin of the logic block and another $V_C$ (load capacitances, column 6, line 50) shows another specific one of the transistor property of the transistor connected to an output pin of the logic block.

10-3. Regarding claims 3 and 9, Iwanishi et al. disclose a method of calculating a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output

pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other (a hot-carrier-delay-degradation method, column 4, line 49, to column5, line 13), comprising the steps of:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect (a delay calculation step, column 4, lines 53-63);

(b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging (a delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b) (an after-deterioration delay calculation step, column 5, lines 9-13).

10-4. Regarding claims 5 and 11, Iwanishi et al. disclose a method of calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks (a hot-carrier-delay-degradation method, column 4, line 49, to column 5, line 16), comprising the steps of:

(a) calculating delay times of all said logic blocks according to the method as in claim 3 or 9 (column 4, line 53 to column 5, line 13); and,

(b) calculating the delay time of the logic level circuit from the result of step (a) (column 5, lines 13-16).

***Allowable Subject Matter***

11. The equations of claims 4, 6, 10, and 12 are not taught exactly by the prior art, and would be allowable if the above rejections under 101 are overcome.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference to Shimizu et al., U.S. Patent 5,615,377 issued March 25, 1997, is cited as teaching a method of simulating hot carrier deterioration of a P-MOS transistor.

Reference to Yonezawa, U.S. Patent 5,974,247 issued October 26, 1999, and filed August 27, 1997, is cited as teaching an apparatus and method of LSI timing degradation simulation.

Reference to Fang et al., U.S. Patent 6,278,964 issued August 21, 2001, and filed May 29, 1998, is cited as teaching a hot carrier effect simulation for integrated circuit.

Reference to Quader et al., "Hot-carrier-reliability design guidelines for CMOS logic circuits", IEEE Journal of Solid-State Circuits, Volume 29, Issue 3, March 1994, pp 253-262, is cited as describing generalized hot-carrier-reliability design rules.

Reference to Minehane et al., "Direct BSIM3v3 parameter extraction for hot-carrier reliability simulation of N-channel LDD MOSFETs", Proceedings of the 1997 6th International Symposium on Physical & Failure Analysis of Integrated Circuits, 1997, pp 133-139, is cited as describing direct parameter extraction procedures.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
May 3, 2002

SAMUEL BRODA, ESQ.
PATENT EXAMINER